This listing of claims will replace all prior versions, and listings, of claims in the present application:

LISTING OF CLAIMS:

Claim 1 (Currently Amended) A memory array comprising:

at least one first-type memory device, each of said at least one first-type memory device comprising a first transistor, a first underlying capacitor, a first buried strap, and a first collar region with a first vertical length which is substantially constant throughout the periphery of said first collar region, wherein said first buried strap is located at a first depth and is positioned on said first collar region and is in electrical contact with both said first transistor and said first underlying capacitor; and

at least one second-type memory device, each of said at least one second-type memory device comprising a second transistor, a second underlying capacitor, an offset buried strap, and a second collar region with a second vertical length which is substantially constant throughout the periphery of said second collar region, wherein said offset buried strap is located at a second depth that is different from said first depth and is positioned on said second collar region and is in electrical contact with both said second transistor and said second underlying capacitor, and said second vertical length is equal to said first vertical length.

Claim 2 (Previously Presented) The memory array of Claim 1 further comprising:

at least one other-type memory device, each of said at least one other-type memory device comprising another transistor, another underlying capacitor, a further-offset buried strap, and

another collar region with another vertical length, wherein said further-offset buried strap is located at another depth that is different from said first depth and from said second depth and is positioned on said another collar region and is in electrical contact with both said another transistor and said another underlying capacitor, and said another vertical length is equal to said first vertical length.

Claim 3 (Original) The memory array of Claim 1, wherein said first buried strap region and said offset buried strap region are offset by a vertical dimension ranging from about 0.4 μm to about 0.6 μm.

Claim 4 (Previously Presented) The memory array of Claim 1, wherein said first underlying capacitor comprises at least one first-bottling region and said second underlying capacitor comprises at least one offset-bottling region, wherein the depth of said at least one first-bottling region is different from the depth of said at least one offset-bottling region.

Claim 5 (Original) The memory array of Claim 1, further comprising a support region.

Claim 6 (Previously Presented) The memory array of Claim 1, wherein said at least one first-type memory device is formed within a first trench and said at least one second-type memory device is formed within a second trench.

Claim 7 (Previously Presented) The memory array of Claim 6, wherein said first trench has a depth ranging from about 1 μm to about 10 μm and said second trench has a depth ranging from about 1 μm to about 10 μm.

Claim 8 (Previously Presented) A memory array comprising:

at least one first-type memory device, each of said at least one first-type memory device comprising a first transistor and a first underlying capacitor that are in electrical contact to each other through a first buried strap, said first buried strap positioned on a first collar region; and

at least one second-type memory device, each of said at least one second-type memory device comprising a second transistor and a second underlying capacitor that are in electrical contact to each other through an offset buried strap, said offset buried strap is located at a depth that is different from the depth of the first buried strap, and is positioned on a second collar region, wherein said second collar region including at least said offset buried strap has a length equal to a length of said first collar region including at least said first buried strap and a first bottom surface of said first collar region is vertically offset from a second bottom surface of said second collar region.

Claim 9 (Original) The memory array of Claim 8 wherein said first bottom surface is vertically offset from said second bottom surface by a dimension ranging from about 0.4 μm to about 0.6 μm.

Claim 10 (Original) The memory array of Claim 1 wherein said first underlying capacitor and said second underlying capacitor have a vertical orientation.

Claims 11-20 (Cancelled)

Claim 21 (Currently Amended) A memory array compris[[es]]ing:

at least one first-type memory device, each of said at least one first-type memory device comprising a first transistor and a first underlying capacitor that are in electrical contact to each other through a first buried strap, said first buried strap positioned on a first collar region; and

at least one second-type memory device, each of said at least one second-type memory device comprising a second transistor and a second underlying capacitor that are in electrical contact to each other through an offset buried strap, said offset buried strap positioned on a second collar region, wherein said second collar region has a length equal to a length of said first collar region and wherein a first bottom surface of said first collar region is vertically offset from a second bottom surface of said second collar region.